XINYU LUO

City University of Hong Kong
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EDUCATION

City University of Hong Kong, Hong Kong *Sep. 2024 - present*
PhD Candidate in Electrical Engineering, expected August 2028

- Supervisor: Haoliang Li, Arindam Basu
- Research Interest: LLM, Transfer Learning, Hardware-software Co-design

Southeast University, Nanjing, China *Sep. 2020 - Jun. 2024*
Bachelor of Information Engineering

- Overall GPA: 3.92/4 Average Score: 91.46/100

PUBLICATIONS

SPACE: SPike-Aware Consistency Enhancement for Test-Time Adaptation in Spiking Neural Networks
Xinyu Luo, Kecheng Chen, Pao-Sheng Vincent Sun, Chris Xing Tian, Arindam Basu, Haoliang Li
Neural Information Processing Systems Conference (NeurIPS), 2025

A 33.6–136.2-TOPS/W Nonlinear Analog Computing-in-Memory Macro for Multi-Bit LSTM Accelerator in 65-nm CMOS
Junyi Yang, **Xinyu Luo**, Ye Ke, Zheng Wang, Hongyang Shang, Shuai Dong, Zhengnan Fu, Xiaofeng Yang, Hongjie Liu, Arindam Basu
IEEE Journal of Solid-State Circuits (JSSC), 2025

Test-time Adaptation for Foundation Medical Segmentation Model without Parametric Updates
Kecheng Chen, **Xinyu Luo**, Tiexin Qin, Jie Liu, Hui Liu, Victor Ho Fun Lee, Hong Yan, Haoliang Li
International Conference on Computer Vision (ICCV), 2025

EXPERIENCE

Research Internship: Big Data Acceleration on FPGAs
July 2023 - October 2023 *Simon Fraser University, Burnaby, Canada*

- I applied to Mitacs Globalink Research Program which is funded by Mitacs and China Scholarship Council, and was selected by Professor Zhenman FANG after three rounds of elimination (200 out of around 20k applicants).
- I optimize codes by consolidating multiple computational digital values within a single DSP operand, thereby effectively leveraging DSP resources, and achieving parallel data calculation, consequently enhancing data processing speed.

PROJECTS

All-digital Phase-locked Loop Based on Counter Architecture
December 2022 - May 2023 *Southeast University*

- In a team of five under Professor Lu TANG's supervision: I proposed an ADPLL model based on counter architecture, which is verified through FPGA simulation. The project was finally rated as 'Excellent'.

HONORS & SCHOLARSHIPS

- Postgraduate Scholarship of City University of Hong Kong
- President Scholarship of Southeast University (3 out of 248)
- 2 times Excellent Student Scholarship of Southeast University (29 out of 248)
- The Second Prize in the Chinese Mathematics Competition
- The Third Prize in the Southeast University Smart Car Competition